Ow # 2825

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
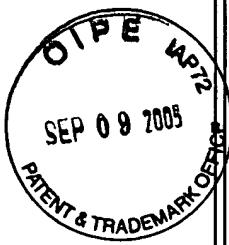
Applicant(s):   Manjunath Haritsa et al.

Assignee: Sun Microsystems, Inc.

Title: SIMULATION BY PARTS METHOD FOR GRID-BASED CLOCK
                DISTRIBUTION DESIGN

Serial No.:   09/982,458   Filed: October 17, 2001

Examiner: Binh C. Tat   Group Art   2825
                                  Unit:

Docket No.:   P-5404

Monterey, CA
September 7, 2005

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT
UNDER §1.97(c) WITH FEE

Sir:

     Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant(s)
wish to call the following documents (a copy of each is
enclosed) to the attention of the Examiner.

U.S. PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	NAME
1)	5,387,885	02/07/95	Chi
2)	5,467,040	11/14/95	Nelson et al.
3)	5,581,473	12/03/96	Rusu et al.
4)	5,644,498	07/01/97	Joly et al.
5)	5,656,963	08/12/97	Masleid et al.
6)	5,778,216	07/07/98	Venkatesh
7)	5,864,487	01/26/99	Merryman et al.
8)	5,896,055	04/20/99	Toyonaga et al.
9)	5,917,729	06/29/99	Naganuma et al.

09/12/2005 EAYALEW1 00000022 09982458
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- 1 -   Serial No. 09/982,458

10)	5,963,729	10/05/99	Aji et al.
11)	5,974,245	10/26/99	Li et al.
12)	5,994,924	11/30/99	Lee et al.
13)	6,088,254	07/11/00	Kermani
14)	6,204,713	03/20/01	Adams et al.
15)	6,205,572	03/20/01	Dupenloup
16)	6,260,182	07/10/01	Mohan et al.
17)	6,263,478	07/17/01	Hahn et al.
18)	6,289,412	09/11/01	Yuan et al.
19)	6,289,498	09/11/01	Dupenloup
20)	6,378,080	04/23/02	Anjo et al.
21)	6,442,740	08/27/02	Kanamoto et al.
22)	6,457,159	09/24/02	Yalcin et al.
23)	2003/0074175	04/17/03	Haritsa et al.
24)	2003/0074643	04/17/03	Schmitt et al.

FOREIGN DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY
1)	WO 95/34036	12/14/95	PCT

OTHER DOCUMENTS

1)	B. Lampson et al., "A Processor for a High-Performance Personal Computer", Seventh Annual Symposium on Computer Architecture, IEEE, pages 146-160, May 1980.
2)	C-S Wu et al., "An Automatic Cell Characterization Environment for Cell-Based Design Methodology", IEEE, pages 326-329, May 1993.
3)	H. Fair et al., "Clocking Design and Analysis for a 600MHz Alpha Microprocessor", IEEE International Solid State Circuits Conference, IEEE, vol. 41, pages 398-399, 473, February 1998. (XP000862228).
4)	J. Burkis, "Clock Tree Synthesis for High Performance ASICs", IEEE, pages 9-8.1 – 9-8.3, August 1991.
5)	P. Larsson et al., "Impact of Clock Slope on True Single Phase Clocked (TSPC) CMOS Circuits", IEEE Journal of Solid-State Circuits, IEEE, Vol. 29, No.6, pages 723-726, June 1994.
6)	P.J. Restle et al., "A Clock Distribution Network for Microprocessors", 2000 Symposium on VLSI Circuits, IEEE, pages 184-187, April 2000.

7)	R.B. Mueller-Thuns et al., "Parallel Switch-Level Simulation for VLSI", _Proceedings of the European Conference on Design Automation_, IEEE, pages 324-328, February 1991. (XP010093616).
8)	S. Boon et al., "High Performance Clock Distribution for CMOS ASICs", _Custom Integrated Circuits Conference_, IEEE, pages 15.4.1 - 15.4.5, May 1989. (XP010082184).
9)	J-S Yim et al., "A Floorplan-based Planning Methodology for Power and Clock Distribution in ASICs", _Proceedings ACM/IEEE Conference on Design Automation_, ACM, pages 766-771, June 1999.

A PTO form 1449 listing these documents is enclosed. Citation of the above documents shall not be construed as:

    1.   an admission that the documents are necessarily prior art with respect to the instant invention;

    2.   a representation that a search has been made, other than as described above; or

    3.   an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

Enclosed herewith is a check in the amount of $180.00 payable to the Director of the United States Patent and Trademark Office, which is the amount for submission of an Information Disclosure Statement given in 37 C.F.R. § 1.17(p).

The Commissioner is hereby authorized to charge any additional fees, which may be required to consider this paper, or credit any overpayment to Deposit Account No. 50-0553.

Respectfully submitted,
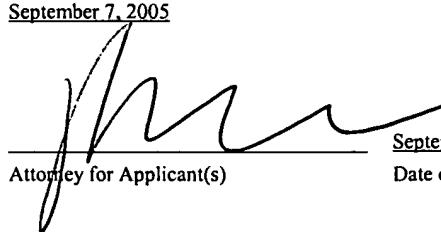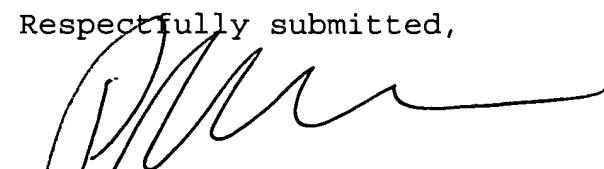
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       Serial No. 09/982,458

Form PTO-1449		Atty Docket No. P-5404	Serial No. 09/982,458

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Applicant(s) Manjunath Haritsa et al.	
Filing Date October 17, 2001	Group 2825

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	5,387,885	02/07/95	Chi	333	100	
	AB	5,467,040	11/14/95	Nelson et al.	327	276	
	AC	5,581,473	12/03/96	Rusu et al.	364	490	
	AD	5,644,498	07/01/97	Joly et al.	364	489	
	AE	5,656,963	08/12/97	Masleid et al.	327	297	
	AF	5,778,216	07/07/98	Venkatesh	395	558	
	AG	5,864,487	01/26/99	Merryman et al.	364	491	
	AH	5,896,055	04/20/99	Toyonaga et al.	327	295	
	AI	5,917,729	06/29/99	Naganuma et al.	364	491	
	AJ	5,963,729	10/05/99	Aji et al.	395	500.06	
	AK	5,974,245	10/26/99	Li et al.	395	500.11	
	AL	5,994,924	11/30/99	Lee et al.	326	93	

FOREIGN PATENT DOCUMENTS

|		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
	AM	WO 95/34036	12/14/95	PCT				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AN	B. Lampson et al., "A Processor for a High-Performance Personal Computer", _Seventh Annual Symposium on Computer Architecture_, IEEE, pages 146-160, May 1980.
	AO	C-S Wu et al., "An Automatic Cell Characterization Environment for Cell-Based Design Methodology", IEEE, pages 326-329, May 1993.
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Examiner	Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

Form PTO-1449					Atty Docket No. P-5404		Serial No. 09/982,458	

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Applicant(s)
Manjunath Haritsa et al.

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U.S. PATENT DOCUMENTS

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	AA	6,088,254	07/11/00	Kermani	365	63	
	AB	6,204,713	03/20/01	Adams et al.	327	295	
	AC	6,205,572	03/20/01	Dupenloup	716	5	
	AD	6,260,182	07/10/01	Mohan et al.	716	12	
	AE	6,263,478	07/17/01	Hahn et al.	716	10	
	AF	6,289,412	09/11/01	Yuan et al.	711	11	
	AG	6,289,498	09/11/01	Dupenloup	716	18	
	AH	6,378,080	04/23/02	Anjo et al.	713	500	
	AI	6,442,740	08/27/02	Kanamoto et al.	716	6	
	AJ	6,457,159	09/24/02	Yalcin et al.	716	6	
	AK	2003/0074175	04/17/03	Haritsa et al.	703	19	
	AL	2003/0074643	04/17/03	Schmitt et al.	716	6	
	AM						

FOREIGN PATENT DOCUMENTS

							Translation	
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	YES	NO
	AN							

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	AO	P.J. Restle et al., "A Clock Distribution Network for Microprocessors", <u>2000 Symposium on VLSI Circuits</u>, IEEE, pages 184-187, April 2000.
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